Instruction Manual

Tektronix

TMS230
MMC2107 Microcontroller Software Support

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www.tektronix.com

Tektronix, Inc., P.O. Box 500, Beaverton, OR 97077

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Table of Contents

Reference

Index

List of Figures

List of Tables

Preface

This instruction manual contains specific information about the TMS230 MMC2107 microcontroller support package and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microcontroller support packages on the logic analyzer for which the TMS230 MMC2107 support was purchased, you will only need this instruction manual to set up and run the support.

If you are not familiar with operating microcontroller support packages, you will need to supplement this instruction manual with information on basic operations to set up and run the support. See Manual Conventions below for more information.

Manual Conventions

This manual uses the following conventions:

- The term “disassembler” refers to the software that disassembles bus cycles into instruction mnemonics and cycle types.
- The phrase “information on basic operations” refers to your logic analyzer online help or a user manual covering the basic operations of microcontroller support.

Contacting Tektronix

Phone	1-800-833-9200*****
Address	Tektronix, Inc. Department or name (if known) 14200 SW Karl Braun Drive P.O. Box 500 Beaverton, OR 97077 USA
Web site	www.tektronix.com
Sales support	1-800-833-9200, select option 1*****
Service support	1-800-833-9200, select option 2*****
Technical support	Email: techsupport@tektronix.com 1-800-833-9200, select option 3***** 1-503-627-2400 6:00 a.m. – 5:00 p.m. Pacific time

*** This phone number is toll free in North America. After office hours, please leave a voice mail message.**
Outside North America, contact a Tektronix sales office or distributor; see the Tektronix web site for a list of offices.

Getting Started

Getting Started

This section contains information on the TMS230 MMC2107 microcontroller support package and on connecting your logic analyzer to your system under test.

Support Package Description

The TMS230 MMC2107 microcontroller support package displays disassembled data from systems based on the Motorola MMC2107 microcontroller.

To use this support efficiently, you need to have the items listed in the information on basic operations and *Motorola Inc., 02/29/00 User manual*, and *Sika Overview Specification rev 1.2*.

Information on basic operations in your logic analyzer online help also contains a general description of the support.

Logic Analyzer Software Compatibility

The floppy disk label on the microcontroller support states the version of logic analyzer software with which this support is compatible.

Logic Analyzer Configuration

The TMS230 MMC2107 support requires a minimum of one 102-channel module.

Requirements and Restrictions

Review the general requirements and restrictions of microcontroller support packages as they pertain to your system under test.

Also review electrical specifications in *Specifications* on page 3–1 as they pertain to your system under test, as well as the following descriptions of other MMC2107 support requirements and restrictions.

System Clock Rate

The operating speeds with which the MMC2107 support can acquire data from the MMC2107 microcontroller are listed on Table 3–1. These specifications were valid at the time this manual was printed. Contact your Tektronix Sales Representative for current information on the fastest devices supported.

NonIntrusive Acquisition Acquiring microcontroller bus cycles is nonintrusive to your system under test. That is, the TMS230 MMC2107 support does not intercept, modify, or present signals back to your system under test.

Disabling the Instruction Cache The cache is not present on the MMC2107 microcontroller. All instruction prefetches are visible on the bus so they can be acquired and displayed disassembled.

Functionality Not Supported

FAST Mode Fast mode is for factory testing only.

Single Chip Mode In Single Chip mode all memory is internal to the chip.

Connecting the Logic Analyzer to Your System Under Test

You can use channel probes, clock probes, and leadsets with a commercial test clip (or adapter) to make connections between the logic analyzer and your system under test.

To connect the probes to MMC2107 signals in your system under test using a test clip, follow these steps:

1. Power off your system under test. It is not necessary to power off the logic analyzer.

CAUTION. *To prevent static damage, handle the microcontroller, the probes, and the logic analyzer module components only in a static-free environment. Static discharge can damage these components.*

Always wear a grounding wrist strap, heel strap, or similar device while handling the microcontroller.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. If you are using a test clip, touch any of the ground pins on the clip to discharge stored static electricity from the test clip.

CAUTION. *To prevent damage to the pins on the microcontroller, place your system under test on a horizontal static-free surface before connecting the test clip.*

3. Use Tables 5–2 through 5–10 beginning on page 5–3 to connect the channel probes to MMC2107 signal pins on the test clip or in your system under test.

Use leadsets to connect at least one ground lead from each channel probe and the ground lead from each clock probe to ground pins on your test clip.

Operating Basics

Setting Up the Support

The information in this section is specific to the operations and functions of the TMS230 MMC2107 microcontroller support on any Tektronix logic analyzer for which it can be purchased.

Before you acquire and display disassembled data, you need to load the support and specify setups for clocking and triggering as described in the information on basic operations in your logic analyzer online help. The microcontroller support provides default values for each of these setups as well as user-definable settings.

Installing the Support Software

NOTE. *Before you install any software, it is recommended that you verify that the microcontroller support software is compatible with the logic analyzer software.*

To install the TMS230 MMC2107 software on your Tektronix logic analyzer, follow these steps:

1. Insert the floppy disk in the disk drive.
2. Click the Windows Start button, point to Settings, and click Control Panel.
3. In the Control Panel window, double-click Add/Remove Programs.
4. Follow the instructions on the screen for installing the software from the floppy disk.

To remove or uninstall software, close all windows, and then follow the above instructions and select Uninstall.

Channel Group Definitions

The software automatically defines channel groups for the support. The channel groups for the TMS230 MMC2107 support are Address, Data, Control, Proc_Mode, ChipSelect, and Misc. The channel group tables begin on page 5–1.

Support Package Setups

The TMS230 MMC2107 software installs the MMC2107 support package setup file.

MMC2107 Setup This setup provides disassembly support. Signals are displayed as they appear electrically on the front side bus.

Clocking

Options The TMS230 MMC2107 support offers a microcontroller-specific clocking mode for the MMC2107 microcontroller. This clocking mode is the default selection whenever you load the TMS230 MMC2107 support.

Disassembly is not correct when using the Internal or External clocking modes. Information on basic operations in your online help describes in more detail how to use these clock selections for general purpose analysis.

- Internal clocking is used for timing and is based on the clock generated by a Tektronix logic analyzer. You can configure the clock rate from 50 ms down to 4 ns resolution.
- External clocking is used when you configure the clocking of data based on logical combinations of clocks and qualifiers.

Custom Clocking

When Custom is selected, the Custom Clocking Options menu has the subtitle MMC2107 microcontroller Clocking Support added, and the clocking option is displayed.

The TMS230 MMC2107 support has one clocking option:

External Bus Interface

The External Bus interface option supports both Emulation mode and Master mode. In Emulation mode the SHS~ signal is enabled by default. For Master mode to function correctly, the SHS~ signal must be enabled.

In Master mode, the SHS~ signal is enabled by writing to the port E pin assignment register (PEPAR).

Figure 2–1 shows the bus timing for External Bus Interface (EBI) Memory Read cycle.

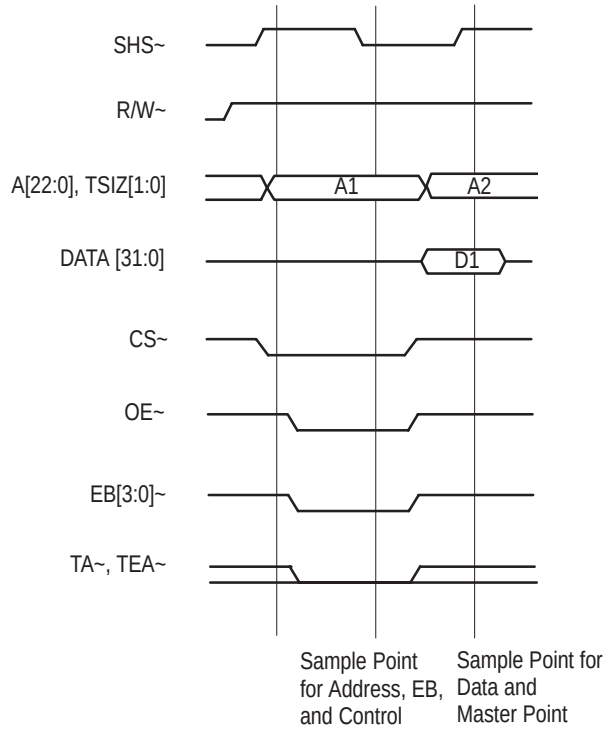

Figure 2–1: Timing diagram of Sample point and Master sample point

Acquiring and Viewing Disassembled Data

Acquiring Data

After you load the TMS230 MMC2107 support, choose a clocking mode, and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your logic analyzer online help or *Appendix A: Error Messages and Disassembly Problems* in your logic analyzer user manual.

Viewing Disassembled Data

You can view disassembled data in six display formats: Timing, State, Hardware, Software, Control Flow, and Subroutine. The information on basic operations describes how to select the disassembly display formats.

NOTE*. Selections in the Disassembly property page (the Disassembly Format Definition overlay) must be set correctly for your acquired data to be disassembled correctly. Refer to* Changing How Data is Displayed *on page 2–8.*

The default display format displays the Address, Data, Control, Proc_Mode, and ChipSelect channel group values for each sample of acquired data along with Sample, Mnemonic, and Timestamp.

Any channel group or display column can be made visible by selecting the Add column option in the Disassembly property page.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2–1 defines these special characters and strings.

Table 2–1: Description of special characters in the display

Character or string	Definition
#	Indicates an immediate value.
>> On the TLA 700	Indicates that the instruction was manually marked as a program fetch.
t	Indicates that the number shown is in decimal, such as #12t.

Timing Display Format

The Timing-Waveform display format file is provided for the TLA 700 Series support. The timing-waveform display format file sets up and displays the following waveforms:

Address (busform)
Data (busform)
R/W~
SHS~
OE~
RST~
EB[0:3]~

Hardware Display Format

In Hardware display format, the disassembler displays certain cycle type labels in parentheses. Table 2–2 lists cycle type labels and gives a definition of the cycle they represent.

Table 2–2: Cycle type labels and definitions

Cycle Type	Definition
(RESET)	Indicates system RESET
(READ)	Indicates DATA READ cycle
(WRITE)	Indicates DATA WRITE cycle
(FLUSH)	Indicates a cycle was fetched but not executed
(UNKNOWN)	Indicates a combination of control bits are unexpected or unrecognized
(ILLEGAL INSTRUCTION)	Indicates parsing errors
(DATA RETRIEVAL ERROR)	Indicates invalid DATA READ cycle

Figure 2–2 shows an example of a Hardware display.

Sample	MMC2107 Address	MMC2107 Data	MMC2107 Mnemonics		MMC2107 Control	MMC2107 ChipSele
7302	81010056	----0145	ZEXTB	R5	READ	1011
7303	81010058	0166----	ZEXTH	R6	READ	1011
7304	8101005A	----F7D2	BR	81010000	READ	1011
7305	8101005C	1254----	(FLUSH)		READ	1011
7306	81010000	7E18----	LRW	R14,[81010060]	READ	1011
7307	81010002	----01E6	ABS	R6	READ	1011
7308	81010060	8101C000	(READ)		READ	1011
7309	81010004	01E7----	ABS	R7	READ	1011
7310	81010006	----01E8	ABS	R8	READ	1011
7311	81010008	7317----	LRW	R3,[81010064]	READ	1011
7312	8101000A	----1230	MOV	R0,R3	READ	1011
7313	81010064	8101C500	(READ)		READ	1011
7314	8101000C	8300----	LD.W	R3,(R0,0x0)	READ	1011
7315	8101000E	----1230	MOV	R0,R3	READ	1011
7316	8101C500	080EBECD	(READ)		READ	1011
7317	81010010	1276----	MOV	R6,R7	READ	1011
7318	81010012	----1298	MOV	R8,R9	READ	1011
7319	81010014	7415----	LRW	R4,[81010068]	READ	1011
7320	81010016	----00D4	JSR	R4	READ	1011
7321	81010068	8101001E	(READ)		READ	1011
7322	81010018	01E6----	(FLUSH)		READ	1011
7323	8101001E	----2470	SUBI	R0,#08	READ	1011
7324	81010020	1232----	MOV	R2,R3	READ	1011
7325	81010022	----F804	BSR	8101002C	READ	1011
7326	81010024	1254----	(FLUSH)		READ	1011
7327	8101002C	1276----	MOV	R6,R7	READ	1011
7328	8101002E	----6015	MOVI	R5,#01	READ	1011
7329	81010030	6006----	MOVI	R6,#00	READ	1011
7330	81010032	----0E65	TST	R5,R6	READ	1011

Figure 2–2: Hardware display format

Software Display Format

The Software display format displays only the first fetch of executed instructions. Flushed cycles and extensions are not shown, even though they are part of the executed instruction. Read extensions are used to disassemble the instruction, but they are not displayed as a separate cycle in the Software display format. Data reads and writes are not displayed.

Control Flow Display Format

The Control Flow display format displays only the first fetch of instructions that cause a branch in the addressing and special cycles to change the flow of control.

Instructions that generate a change in the flow of control in the MMC2107 microcontroller are as follows:

BR	Branch
JMP	Jump
JMPI	Jump indirect

Instructions that may generate a change in the flow of control in the MMC2107 microcontroller are as follows:

BT	Branch on condition True
BF	Branch on condition False

Subroutine Display Format

The Subroutine display format displays only the first fetch of subroutine call or return instructions. It can display conditional subroutine calls if they are considered to be taken.

Instructions that generate a subroutine call or a return in the MMC2107 microcontroller are as follows:

BSR	Branch on subroutine
JSR	Jump to subroutine
JSRI	Jump to subroutine indirect

Changing How Data is Displayed

Common fields and features allow you to further modify displayed data to suit your needs. You can make common and optional display selections in the Disassembly property page (the Disassembly Format Definition overlay).

Optional Display Selections

You can make optional selections for acquired disassembled data. In addition to the common selections (described in the information on basic operations), you can change the displayed data in the following ways:

Show:	Hardware	(default)
	Software	
	Control Flow	
	Subroutine	
Highlight:	Software	(default)
	Control Flow	
	Subroutine	
	None	
Disasm Across Gaps:		No (default)
		Yes

Micro-Specific Fields

Data Port Width. Indicate the data port width:

32 bit port	(default)
16 bit port	

NOTE. *The 16 bit port is assigned to pins D[31:16] and the 32 bit is assigned to pins D[31:0].*

Base Address. You can enter the Base Address of the Memory map from your system under test in the Base Address field in the Disassembly Properties page.

CS0 Base Address
CS1 Base Address
CS2 Base Address
CS3 Base Address

For example, CS2~ is mapped to 0x81000000, enter this address in CS2 Base Address field. Each ChipSelect signal, CS0~ to CS3~, is mapped to a memory of 8 MB in size.

Marking Cycles

The TMS230 MMC2107 support allows marks on potential instruction fetch cycles (which includes read extensions and flush cycles.) Cycle marks are not available if the cursor is placed on other cycle marks. To place a cycle mark use the Mark Opcode button. The Mark Opcode button functions when disassembly is available.

If the cycle being marked is not a potential instruction fetch cycle (which includes read extensions and flush cycles), the Mark Opcode selections are replaced by a note indicating that “An Opcode Mark cannot be placed at the selected data sample.”

When a cycle is marked, this character, >>, is displayed immediately to the left of the Mnemonics column. Cycles can be unmarked by using the Undo Mark selection, which removes this character, >>. If more than one set of sequences are marked, then the you can undo the marks using the Remove all Marks option.

The following cycle marks are available for instruction fetch cycles in the 16 bit Data Port:

Opcode	Marks the cycle as an instruction opcode
Flush	Marks the cycle as a flushed cycle
Undo Mark	Removes all marks from the current sample

The following cycle marks are available for instruction fetch cycles in the 32 bit Data Port:

Opcode	Marks the cycle as an instruction opcode
Opcode_Flush	The first 16 bits are decoded and the lower 16 bits are flushed
Flush_Opcode	The first 16 bits are flushed and the lower 16 bits are decoded
Flush	Marks the cycle as a flushed cycle
Undo Mark	Removes all marks from the current sample

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided on your TMS230 MMC2107 software support disk so you can see an example of how your MMC2107 microcontroller bus cycles and instruction mnemonics look when they are disassembled. Viewing the system file is not a requirement for preparing the module for use. You can view the system file without connecting the logic analyzer to your system under test.

Specifications

Specifications

This section contains information regarding the specifications of the TMS230 MMC2107 microcontroller support.

Specification Tables

Table 3–1 lists the electrical requirements that the system under test must produce for the TMS230 MMC2107 support to acquire correct data.

Table 3–1: Electrical specifications

Characteristics	Requirements
System under test clock rate	
Maximum specified clock rate	33 MHz
Tested clock rate *	33 MHz
Minimum setup time required	2.5 ns
Minimum hold time required	0 ns

*** Contact your Tektronix Sales Representative for current information on the tested clock rate.**

Replaceable Parts

Replaceable Parts

This section contains a list of the replaceable components for the TMS230 MMC2107 support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Using the Replaceable Parts List

The tabular information in the Replaceable Parts List is arranged for quick retrieval. Understanding the structure and features of the list helps you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
TK2548	XEROX CORPORATION	14181 SW MILLIKAN WAY	BEAVERTON, OR 97005

Replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
					STANDARD ACCESSORIES		
	071-0894-00			1	MANUAL, TECH: INSTRUCTIONS, MC210, TMS230	TK2548	071-0894-00

Reference

Reference: Tables

This section lists the Symbol table and the Channel group tables for disassembly and timing.

Symbol Table

Table 5–1 lists the name, bit pattern, and meaning for the symbols in the file MMC2107_Ctrl, the Control channel group symbol table.

Table 5–1: MMC2107 _Ctrl group symbol table definitions

Symbol	Control group value										Meaning
	RST~	TEA~	R/W~	INT7~	INT6~	OE~	EB3~	EB2~	EB1~	EB0~	
RESET	0	X	X	X	X	X	X	X	X	X	RESET
DATA_RETR_ERR	1	0	X	X	X	X	X	X	X	X	Data Retrieval Error
WRITE	1	1	0	X	X	X	X	X	X	X	Data Write
READ	1	1	1	X	X	X	X	X	X	X	Data Read
UNKNOWN	X	X	X	X	X	X	X	X	X	X	Unknown

Channel Assignments

Channel assignments listed in Tables 5–2 through 5–7 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are listed starting with the most significant bit (MSB), descending to the least significant bit (LSB).
- Channel group assignments are for all modules unless otherwise noted.
- A tilde symbol (~) following a support channel name indicates an active low signal.
- An equals symbol (=) following a support channel name indicates that it is double probed.
- The module in the lower-numbered slot is referred to as the Master module and the module in the higher-numbered slot is referred to as the Slave module.

  The portable logic analyzer has the lower-numbered slots on the top, and the benchtop logic analyzer has the lower-numbered slots on the left.

The channel assignment groups are displayed on screen in the following order:

Group name	Display radix
Address	Hexadecimal
Data	Hexadecimal
Mnemonic	None
Control	Symbolic
ChipSelect	BIN
Proc_Mode	BIN
Misc	Off

Table 5–2 lists the probe section and channel assignments for the Address group and the microcontroller signal to which each channel connects. By default the Address channel group assignments are displayed in hexadecimal.

Table 5–2: Address channel group assignments

Bit order	Section:channel	MMC2107 support channel name
31	A3:7	CS0~
30	A3:6	CS1~
29	A3:5	CS2~
28	A3:4	CS3~
27	A3:3	CSE0
26	A3:2	CSE1
25	A3:1	Not used
24	A3:0	Not used
23	A2:7	Not used
22	A2:6	A22
21	A2:5	A21
20	A2:4	A20
19	A2:3	A19
18	A2:2	A18
17	A2:1	A17
16	A2:0	A16
15	A1:7	A15
14	A1:6	A14
13	A1:5	A13
12	A1:4	A12
11	A1:3	A11
10	A1:2	A10
9	A1:1	A9
8	A1:0	A8
7	A0:7	A7
6	A0:6	A6
5	A0:5	A5
4	A0:4	A4
3	A0:3	A3
2	A0:2	A2
1	A0:1	A1
0	A0:0	A0

Table 5–3 lists the probe section and channel assignments for the Data group and the microcontroller signal to which each channel connects. By default the Data channel group assignments are displayed in hexadecimal.

Table 5–3: Data channel group assignments

Bit order	Section:channel	MMC2107 support channel name
31	D3:7	D31
30	D3:6	D30
29	D3:5	D29
28	D3:4	D28
27	D3:3	D27
26	D3:2	D26
25	D3:1	D25
24	D3:0	D24
23	D2:7	D23
22	D2:6	D22
21	D2:5	D21
20	D2:4	D20
19	D2:3	D19
18	D2:2	D18
17	D2:1	D17
16	D2:0	D16
15	D1:7	D15
14	D1:6	D14
13	D1:5	D13
12	D1:4	D12
11	D1:3	D11
10	D1:2	D10
9	D1:1	D9
8	D1:0	D8
7	D0:7	D7
6	D0:6	D6
5	D0:5	D5
4	D0:4	D4
3	D0:3	D3
2	D0:2	D2
1	D0:1	D1
0	D0:0	D0

Table 5–4 lists the probe section and channel assignments for the Control group and the microcontroller signal to which each channel connects. The default radix of the Control group is symbolic on the logic analyzer. The symbol table file name is MMC2107_Ctrl.

Table 5–4: Control channel group assignments

Bit order	Section:channel	MMC2107 support channel name
9	C2:3	RST~
8	Qual:1	TEA~
7	Clock:1	R/W~
6	C3:3	INT7~
5	C3:2	INT6~
4	Clock:3	OE~
3	C0:4	EB3~
2	C0:5	EB2~
1	C0:6	EB1~
0	C0:7	EB0~

ChipSelect channel group assignments listed in Table 5–5 are displayed as binary.

Table 5–5: ChipSelect channel group assignments

Bit order	Section:channel	MMC2107 support channel name
3	A3:4	CS3~
2	A3:5	CS2~
1	A3:6	CS1~
0	A3:7	CS0~

Table 5–6 lists the probe section and channel assignments for the Proc_Mode group and the microcontroller signal to which each channel connects. The default radix of the Proc_Mode group is binary on the logic analyzer.

Table 5–6: Proc_Mode channel group assignments

Bit order	Section:channel	MMC2107 support channel name
6	C2:7	INT5~
5	C2:6	INT4~
4	C2:5	INT3~

Table 5–6: Proc_Mode channel group assignments (cont.)

Bit order	Section:channel	MMC2107 support channel name
3	C2:4	INT2~
2	C3:6	TC2
1	C3:5	TC1
0	C3:4	TC0

Misc channel group assignments listed in Table 5–7 are acquired but not displayed by default.

Table 5–7: Misc channel group assignments

Bit order	Section:channel	MMC2107 support channel name
5	Clock:2	SHS~
4	Qual_1	TA~
3	C1:1	RSTOUT~
0	A3:3	CSE1
0	A3:2	CSE0
1	Clock:1	CLKOUT
0	C1:6	INT0~
0	C1:5	INT1~

Table 5–8 lists the probe section and clock and qualifier channel assignments. The clock probes are not part of any group.

Table 5–8: Clock and Qualifier channel assignments

Section:channel	MMC2107 support channel name	Comments
CLK:0	CLKOUT	–
CLK:1	R/W~	–
CLK:2	SHS~	–
CLK:3	OE~	–
C2:0	Not used	–
C2:1	Not used	–
C2:2	Not used	–
C2:3	RST~	–
QUAL:0	TA~	102 & 136 channel

Table 5–8: Clock and Qualifier channel assignments (cont.)

Section:channel	MMC2107 support channel name	Comments
QUAL:1	TEA~	102 & 136 channel
QUAL:2	Not used	136 channel only
QUAL:3	Not used	136 channel only

Acquisition Setup. The TMS230 MMC2107 support affects the logic analyzer setup menus (and submenus) by modifying existing fields and adding micro-specific fields.

The TMS230 MMC2107 support adds the selection MMC2107 to the Load Support Package dialog box, under the File pulldown menu. After the MMC2107 support is loaded, the Custom clocking mode selection in the module Setup menu is enabled.

Table 5–9 lists the signals required for Clock and Disassembly.

Table 5–9: Signals required for clocking and disassembly

Section:channel	MMC2107 support channel name
R/W~	Clock:1
SHS~	Clock:2
OE~	Clock:3
RST~	C2:3
A22–A0 (Address Group)	A2:6–0
–	A1:7–0
–	A0:7–0
D31–D0 (Data Group)	D3:7–0
–	D2:7–0
–	D1:7–0
–	D0:7–0
EB0~–EB3~	C0:7–4

Table 5–10 lists the signals not required for Clock and Disassembly.

Table 5–10: Signals not required for clocking and disassembly

Section:channel	MMC2107 support channel name
INT5~–INT2~	C2:7–4
CS3~–CS0~	A3:4–7
TC2–TC0	C3:6–4
CLKOUT	CLOCK:0
TA~	QUAL:0
RSTOUT~	C1:1

CPU To Mictor Connections

To probe the microcontroller you need to make connections between the CPU and the Mictor pins of the P6434 Mass Termination Probe. Refer to the *P6434 Mass Termination Probe* manual, Tektronix part number 070-9793-xx, for more information on mechanical specifications. Tables 5–11 through 5–13 list the CPU pin to Mictor pin connections.

Tektronix uses a counterclockwise pin assignment. Pin 1 is located at the top left and pin 2 is located directly below it. Pin 20 is located on the bottom right and pin 21 is located directly above it.

AMP uses an odd side-even side pin assignment. Pin 1 is located at the top left and pin 3 is located directly below it. Pin 2 is located on the top right and pin 4 is located directly below it (see Figure 5–1).

NOTE. *When designing Mictor connectors into your system under test, always follow the Tektronix pin assignment.*

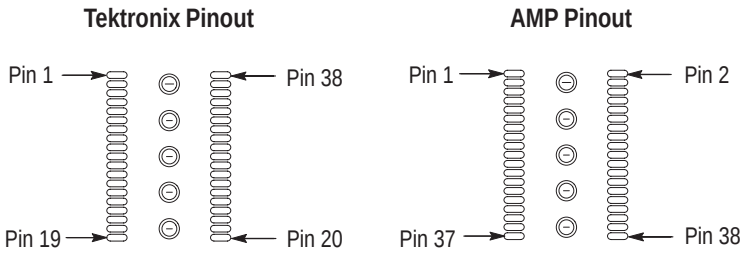

Figure 5–1: Pin assignments for a Mictor connector (component side)

CAUTION. *To protect the CPU and the inputs of the module, it is recommended that a 180 Ω resistor be connected in series between each ball pad of the CPU and each pin of the Mictor connector. The resistor must be within 1/2 inch of the ball pad of the CPU.*

Table 5–11: CPU to Mictor connections for clock and qualifiers

LA channel	MMC2107 support channel name	Tektronix mictor C pin number	AMP mictor C pin number
Clock:3	OE~	C3	C5
Clock:2 CLK	SHS~	D36	D6
Clock:1	R/W~	A36	A6
Clock:0	CLKOUT	A3	A5
C2:3 QUAL	RST~	A16	A31
QUAL:1	TEA~	C36	C6
QUAL:0	TA~	D3	D5

Table 5–12: CPU to Mictor connections for Mictor A pins

Logic analyzer channel	MMC2107 support channel name	Tektronix mictor A pin number	AMP mictor A pin number
A3:7	CS0~	A4	A7
A3:6	CS1~	A5	A9
A3:5	CS2~	A6	A11
A3:4	CS3~	A7	A13
A3:3	CSE0	A8	A15
A3:2	CSE1	A9	A17
A2:6	A22	A13	A25
A2:5	A21	A14	A27
A2:4	A20	A15	A29
A2:3	A19	A16	A31
A2:2	A18	A17	A33
A2:1	A17	A18	A35
A2:0	A16	A19	A37
A1:7	A15	A35	A8
A1:6	A14	A34	A10
A1:5	A13	A33	A12
A1:4	A12	A32	A14
A1:3	A11	A31	A16

Table 5–12: CPU to Mictor connections for Mictor A pins (cont.)

Logic analyzer channel	MMC2107 support channel name	Tektronix mictor A pin number	AMP mictor A pin number
A1:2	A10	A30	A18
A1:1	A9	A29	A20
A1:0	A8	A28	A22
A0:7	A7	A27	A24
A0:6	A6	A26	A26
A0:5	A5	A25	A28
A0:4	A4	A24	A30
A0:3	A3	A23	A32
A0:2	A2	A22	A34
A0:1	A1	A21	A36
A0:0	A0	A20	A38

Table 5–13: CPU to Mictor connections for Mictor D pins

LA channel	MMC2107 support channel name	Tektronix mictor D pin number	AMP mictor D pin number
D3:7	D31	D4	D7
D3:6	D30	D5	D9
D3:5	D29	D6	D11
D3:4	D28	D7	D13
D3:3	D27	D8	D15
D3:2	D26	D9	D17
D3:1	D25	D10	D19
D3:0	D24	D11	D21
D2:7	D23	D12	D23
D2:6	D22	D13	D25
D2:5	D21	D14	D27
D2:4	D20	D15	D29
D2:3	D19	D16	D31
D2:2	D18	D17	D33

Table 5–13: CPU to Mictor connections for Mictor D pins (cont.)

LA channel	MMC2107 support channel name	Tektronix mictor D pin number	AMP mictor D pin number
D2:1	D17	D18	D35
D2:0	D16	D19	D37
D1:7	D15	D35	D8
D1:6	D14	D34	D10
D1:5	D13	D33	D12
D1:4	D12	D32	D14
D1:3	D11	D31	D16
D1:2	D10	D30	D18
D1:1	D9	D29	D20
D1:0	D8	D28	D22
D0:7	D7	D27	D24
D0:6	D6	D26	D26
D0:5	D5	D25	D28
D0:4	D4	D24	D30
D0:3	D3	D23	D32
D0:2	D2	D22	D34
D0:1	D1	D21	D36
D0:0	D0	D20	D38

Table 5–14: CPU to Mictor connections for Mictor C pins

LA channel	MMC2107 support channel name	Tektronix mictor C pin number	AMP mictor C pin number
C3:6	TC2	C5	C9
C3:5	TC1	C6	C11
C3:4	TC0	C7	C13
C3:3	INT7~	C8	C15
C3:2	INT6~	C9	C17
C2:7	INT5~	C12	C23
C2:6	INT4~	C13	C25

Table 5–14: CPU to Mictor connections for Mictor C pins (cont.)

LA channel	MMC2107 support channel name	Tektronix mictor C pin number	AMP mictor C pin number
C2:5	INT3~	C14	C27
C2:4	INT2~	C15	C29
C2:3 *	RST~	C16	C31
C1:6	INT0~	C34	C10
C1:5	INT1~	C33	C12
C1:1	RSTOUT~	C29	C20
C0:7	EB0~	C27	C24
C0:6	EB1~	C26	C26
C0:5	EB2~	C25	C28
C0:4	EB3~	C24	C30

*** Indicates that the channel is a qualifier**

Index

Index

I

L

M

P

R

S

T

U

V

W